HL1361CP00-Ln

DFB Laser Diode Chip

Sample Categories and Disclaimer

Functional sample that has the suffix of "-F" or "-Fx" to the product number is a sample that is designed according to the customer's request. The purpose of this sample is to check and confirm the product feasibility. Thus the sample may be an R&D prototype or may be a modified current product. This sample may not be manufactured in qualified production lines nor using qualified parts. Basically Oclaro guarantees the requested performance of BOL (Beginning Of Life). Any qualification will not be applied.

DESCRIPTION

General

The HL1361CP00-Ln is an LR4 CWDM 1271/1291/1311/1331 nm Distributed Feed-Back (DFB) laser diode chip. Individual chip is designed for 10Gbit/s operation and for use in the dry N2 hermetic sealed package.

PN*	LR4 lane	Wavelength** (nm)	Notes
HL1361CP00-L0	0	1271	For MP use
HL1361CP00-L1	1	1291	
HL1361CP00-L2	2	1311	
HL1361CP00-L3	3	1331	
HL1361CP00-L0-F	0	1271	For initial samples
HL1361CP00-L1-F	1	1291	
HL1361CP00-L2-F	2	1311	
HL1361CP00-L3-F	3	1331	

** Actual wavelength range is specified separately.

Pin Configurations

Fig 1. Block Diagram (one LD chip)

Table 1. Pin Configurations

Pin #	Description	Remarks
1	Laser anode (P electrode)	
2	Laser cathode (N electrode)	

MECHANICAL DIMENSIONS

Individual chip size is 250 μm x 200 μm x 92 μm. Fig. 4 shows a chip outline and metallization pattern. The Anode has typ. 0.55um Au film and Cathode has typ. 0.57um Au film respectively.

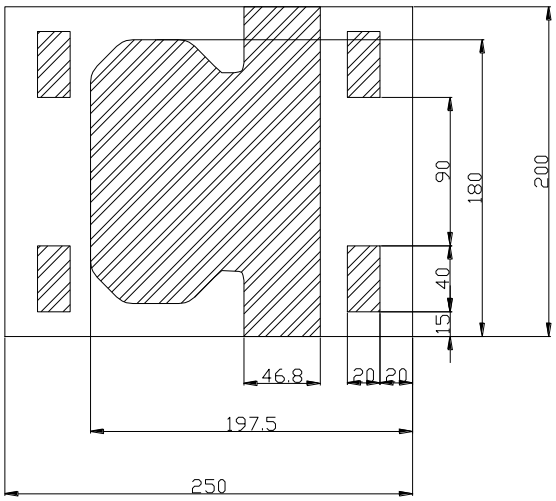


Fig.2 Top view (Anode)

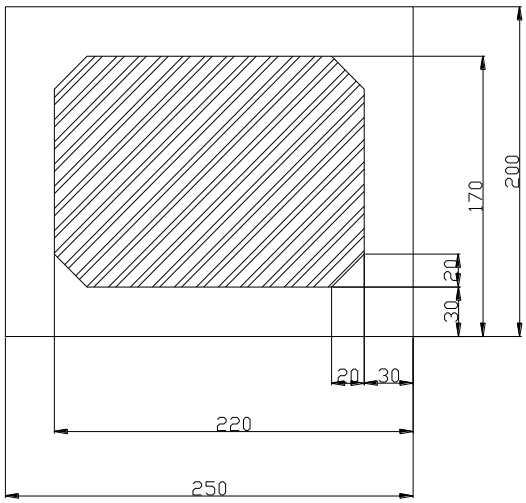
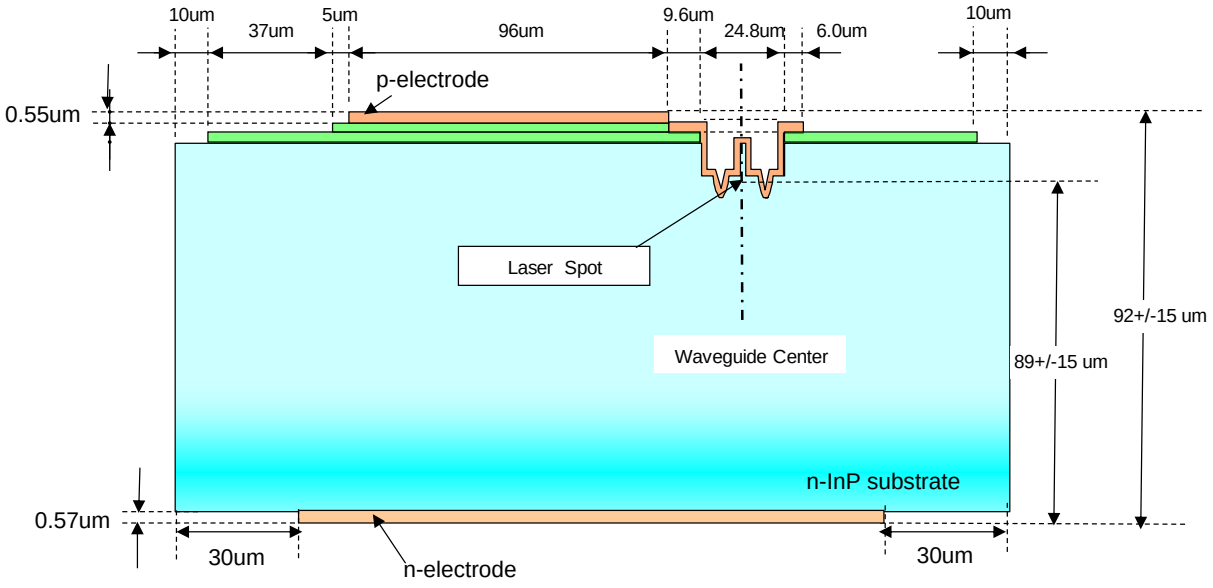


Fig.3 Bottom view (Cathode)

Light output direction



Front facet

(Outline: +/-20um)

Fig 4 Chip Outline and Dimensions

PERFORMANCE SPECIFICATIONS

Absolute Maximum Ratings

Since the HL1361CP00-Ln is a chip form, the performance will depend on not only chip performance but also its assembling process. If the chip is assembled in a proper way, the performance described in Table 2 can be expected but these are not guaranteed values. Oclaro assumes no responsibility for those reliability when they are assembled and/or tested in customer Tc means submount temperature when the chip mounted on Oclaro standard sub-mount soldered on heat sink.

Table 2. Absolute Maximum Ratings (Tc=25°C, unless otherwise specified)

	Absolute Maximum Rating	Min	Max	Unit	
1	Storage temperature	-40	85	C	
2	Operating temperature	-40	95	C	
3	Laser forward bias current	-	150	mA	
4	Laser reverse bias voltage	-	2	V	
5	Die binding temperature	-	350	C	(< 4 s) Note

Note: Recommended condition: 320 C max and 4 s max.

Optical and Electrical Characteristics

Since the HL1361CP00-Ln is a chip form, the performance will depend on not only chip performance but also its assembling process. If the chip is assembled in a proper way, the performance described in Table 3 can be expected but these are not guaranteed values.

Table 3. Expected Optical and Electrical Characteristics

(Tc= -5C to 85C, unless otherwise specified, Condition at CoC (Chip on testing carrier))

No	Optical and Electrical Characteristics	Min	Typ	Max	Units	Notes
1	Lane wavelength range	1264.5 - 1277.5 1284.5 - 1297.5 1304.5 - 1317.5 1324.5 - 1337.5			nm	
2	Lane wavelength range at 25 C	1269±1.5 1289±1.5 1309±1.5 1329±1.5			nm	@ 25C I=33mA
3	Wavelength temperature coefficient		0.1	0.11	nm/degC	
4	Side-mode suppression ratio (SMSR),	35	-	-	dB	@1 C I=33mA @85 C I=70mA
5	Threshold current	-	8	15	mA	@ 25C
		-	20	28	mA	@ 95C
6	Slope efficiency,	-	0.3	-	W/A	@ 25C I=Ith+5mA to Ith+50mA
		0.11	-	-	W/A	@ 95C I=Ith to 70mA
7	Mask Margin (IEEE 10.3Gb/s)	20	-	-	%	@25C I=Ith+25mA PRBS=2^{31}-1, 1k waveforms ER=4.5dB
8	Effective serial resistance	-	7	-	Ohms	@ 95C I=50mA
9	Laser forward voltage	-	1.5	2.0	V	@ 95C I=70mA
10	Kink deviation	-	-	20	%	I=Ith+5 to 100mA See figure 5
11	Far field divergence, Vertical ,	-	35	45	degrees	@ 95C I=70mA
12	Far field divergence, Horizontal,	-	32	40	degrees	@ 95C I=70mA

Note: Tc means sub-mount temperature when the chip mounted on Oclaro standard sub-mount soldered on a heat sink.

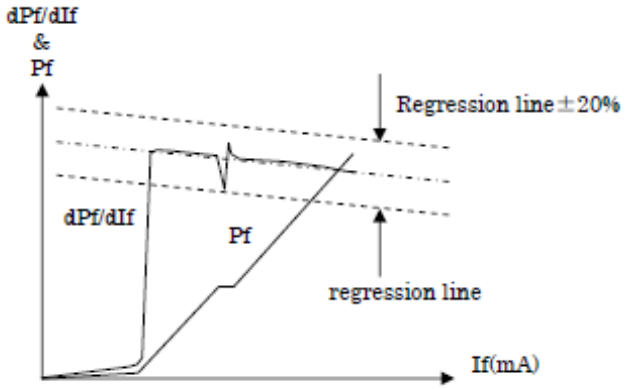


Fig 5 Kink definition

Chip Test Specification

Oclaro (supplier) will perform 100% probe testing on the chips described in Table 4 below. Only chips that pass the criteria in Table 4 will be shipped. The test will be done in bar or chip form using pulsed driving current.

Although chips pass the criteria described in Table 4, Oclaro assumes no responsibility for those performance, yield and reliability when they are assembled and/or tested in customer (buyer). Ts means stage temperature in pulse chip test.

Table 4 Chip test criteria

No.	Parameter	Symbol	Condition	Min	Max	Unit	Remark
1	Threshold current	I_{th}	T_s=85°C	-	21.5	mA	Note1
2	Slope efficiency	Eta	T_s=85°C, I_F=67.5mA	0.087	-	W/A	Note2
3	Peak wavelength (L0)	λ_p	T_s=25°C I_F=67.5mA	1268.7	1271.7	nm	
	Peak wavelength (L1)		T_s=25°C I_F=67.5mA	1288.8	1291.8	nm	
	Peak wavelength (L2)		T_s=25°C I_F=67.5mA	1309.0	1312.0	nm	
	Peak wavelength (L3)		T_s=25°C I_F=67.5mA	1329.3	1332.3	nm	
4	Side mode suppression ratio	SMSR	T_s=25°C I_F=67.5mA	35	-	dB	
			T_s=85°C I_F=67.5mA	35	-	dB	

Note 1 21.5 mA=28 mA x A, A= Temperature correlated factor 0.782
Note 2 0.087 W/A=0.11W/A x B, B= Tester correlated factor 0.792

Wafer Verification Test

Oclaro will perform hard screening (Burn-In), DC measurement and AC measurement using chips mounted on Oclaro standard submount soldered on heat sink. Only the chips that passed the criteria described in this "Wafer Verification Test" section will be used. Only the chips from wafers meeting the minimum yield described in Table 5 will be shipped.

Table 5 Criteria in wafer verification test

Parameter	Condition	Pass Criterion	Minimum Number or Yield
LD chip mount	-	-	20pcs
Start Burn-In test			
Optical Purge test	25°C, 120mA, ACC 3min.	$\|\Delta I_{th}\| \leq +5\%$, $\|\Delta Po\| \leq +10\%$, $\|\Delta Eta\| \leq +10\%$.	
Electrical Purge test	100°C, 150mA, ACC 20h	-	
APC Test	95°C, 70mA, APC 100h, (I_{op}@100h-I_{op}@0h/I_{op}@0h	$-2\% \leq \Delta I_{op} \leq$ **+0.5**%	
Pass Burn-In test			
Start DC test			
Threshold current	T_c=95°C	$I_{th} \leq 28$mA	
Slope efficiency	T_c=95°C, Eta≡Po(70mA)/(70mA-I_{th})	Eta≥0.11W/A	
Forward voltage	T_c=1°C, I_o=33mA T_c=95°C, I_o=70mA	$V_{op} \leq 1.8$V	
Kink deviation,	T_c=1°C and 95℃, Ith+5 to 100mA	kink free	
Peak wavelength L0	T_c=1°C, I_o=33mA	1265.2nm≤λp≤1277.5nm	
	T_c=95°C, I_o=70mA	1265.2nm≤λp≤1277.5nm	
L1	T_c=1°C, I_o=33mA	1285.2nm≤λp≤1297.5nm	
	T_c=95°C, I_o=70mA	1285.2nm≤λp≤1297.5nm	
L2	T_c=1°C, I_o=33mA	1305.2nm≤λp≤1317.5nm	
	T_c=95°C, I_o=70mA	1305.2nm≤λp≤1317.5nm	
L3	T_c=1°C, I_o=33mA	1325.2nm≤λp≤1337.5nm	
	T_c=95°C, I_o=70mA	1325.2nm≤λp≤1337.5nm	
Side mode suppression ratio	T_c=1℃, Io=33mA T_c=95°C, I_o=70mA	SMSR≥35dB	
Beam divergence angle (Horizontal)	T_c=95°C, I_o=70mA	FWHM_H≤36deg	
Beam divergence angle (Vertical)	T_c=95°C, I_o=70mA	FWHM_V≤40deg	
Pass DC test			10 of 20pcs (50%)

OTHER SPECIFICATIONS

Packing and label

The products will be packed as described in Fig. 6 below.

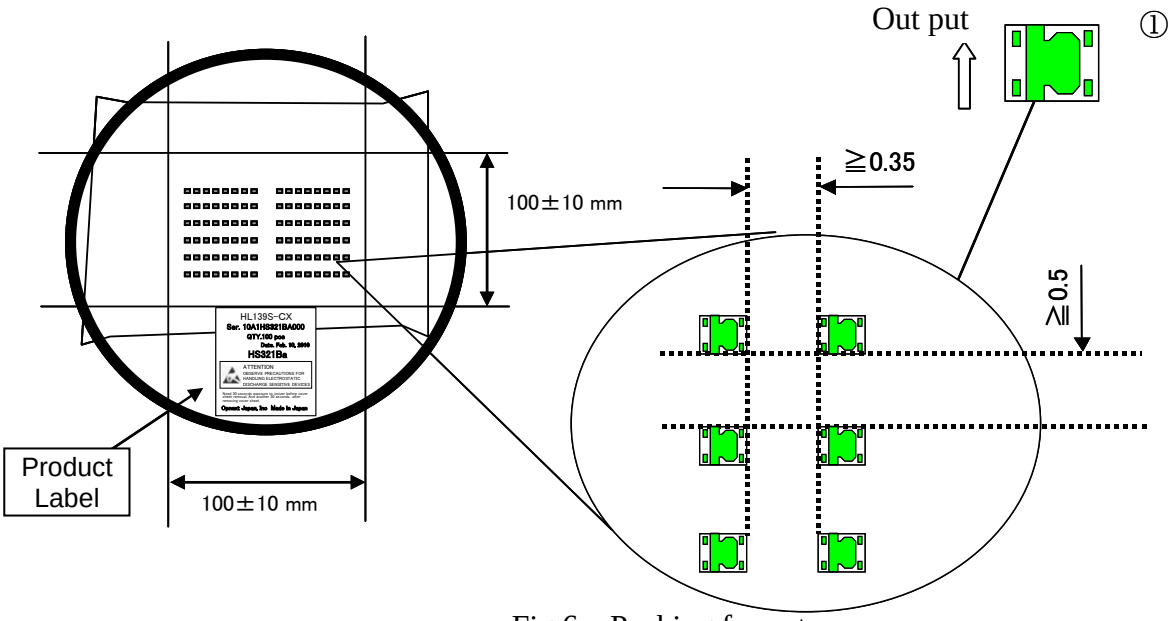


Fig 6 Packing format

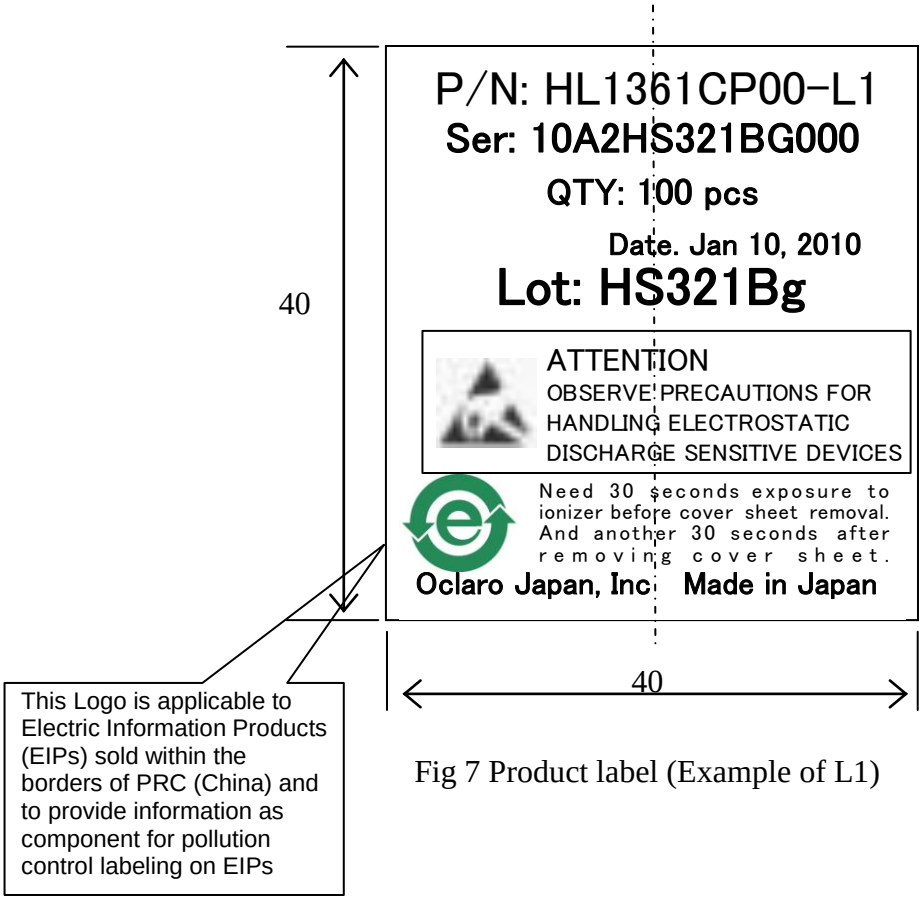


Fig 7 Product label (Example of L1)

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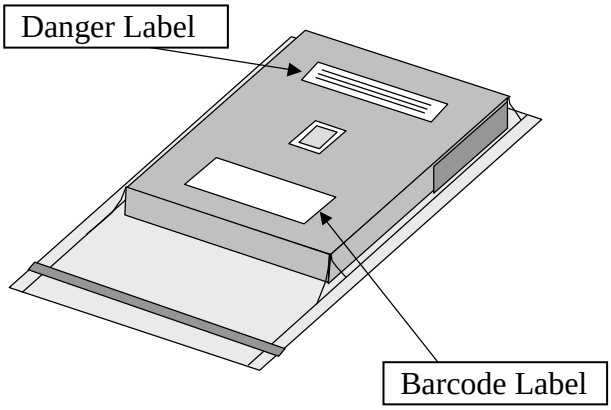

The plastic bag is vacuum-packed.

Fig 8 Packing bag (Example)

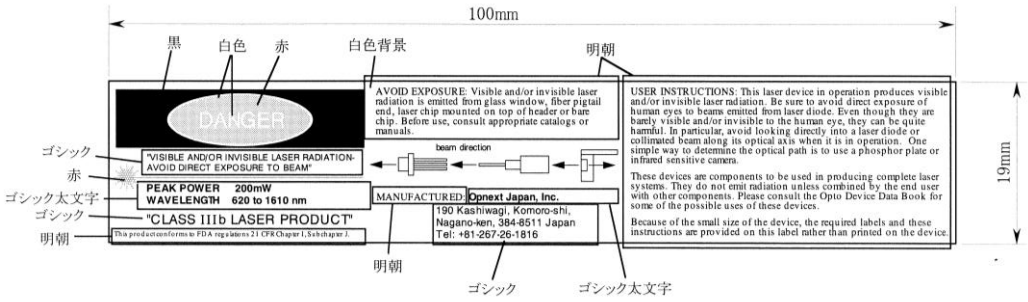

Fig 9 Danger Label (Example)

Bar code label is on plastic bag for each shipment form. Supplier Product Name, Supplier lot number, the Quantity and Customer Part Number are on it. Please see Fig.8. 40x 80 mm

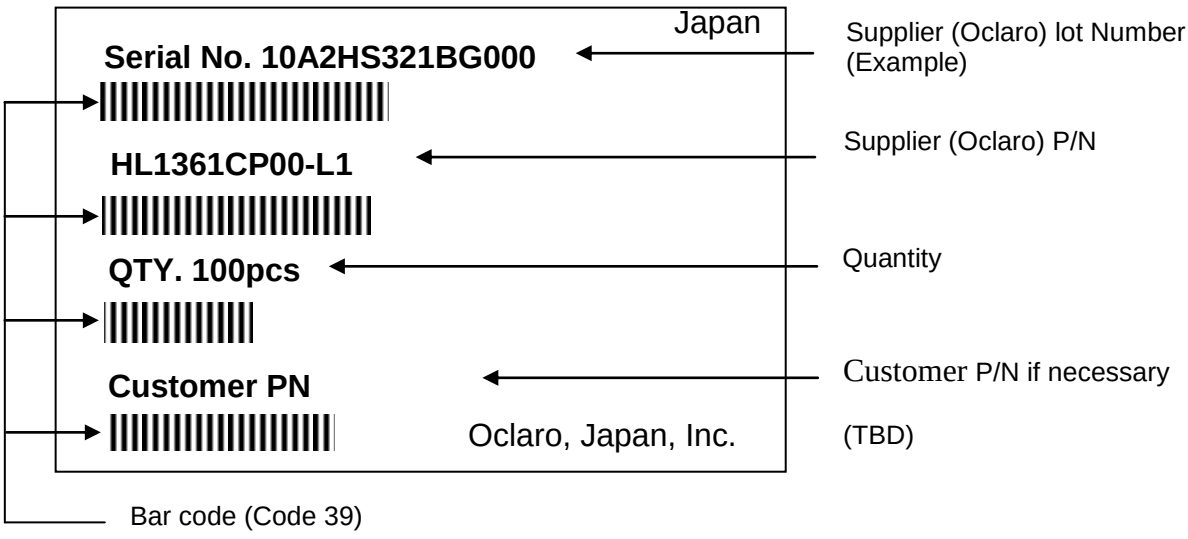

Fig. 10 Bar code label on outer plastic bag (Example of HL1361CP00-L1)

Revision History

Rev.	Date	Page/Line/Fig/Table	Modification	Note
0.0	Nov. 20th, 2014			